What Is Claimed Is:

1. A method of processing signals of a timing controller of a liquid crystal display module, comprising the steps of:

(a) receiving a data enable signal DE which has a vertical blank period;

(b) generating a gate clock signal CPV which has a plurality of gate clock cycles C1-Cn;

(c) generating a plurality of gate-on enable signals OE simultaneously according to the plurality of gate clock cycles C1-Cn of the gate clock signal CPV; and

(d) generating start vertical signals STV before the end of the vertical blank period VB and after at least a gate clock cycle C1 during the vertical blank period VB.

2. The method as claimed in claim 1, wherein in the step (c), start vertical signals STV are generated after at least a third cycle C3 during the vertical blank period VB.

3. The method as claimed in claim 1, after the step (d) further comprising a step of:

pausing outputting CPV, STV, and OE till the end of the vertical blank period VB.

4. The method as claimed in claim 1, wherein the start vertical signals STV includes:

a first start vertical signal STV1, for determining a start scan location of a frame; and

a second start vertical signal STV2, for offsetting flicker and display brightness of the liquid crystal display .

5. The method as claimed in claim 1, wherein the start vertical signals STV uses only a first start vertical signal STV1 to determine a start scan location of a frame;